WHAT IS CLAIMED IS:

1. A field effect transistor for detecting a magnetic field comprising:

   a doped layer;

   doped source and drain regions formed in said doped layer, said doped layer defining a lengthwise extending channel between said source and drain regions;

   first and second drain contacts spaced laterally relative to the length of said channel interconnected with said drain region;

   a gate proximate said channel, for controlling current that may flow from said source to said drain region;

   first and second supplemental gates, spaced laterally relative to the length of said channel, said first and second supplemental gates electrically isolated from each other and said gate, wherein a potential difference between said first and second supplemental gates exerts a lateral electric field in said channel.

2. The field effect transistor of claim 1, wherein said first drain portion and said first supplemental gate are located laterally proximate a first lateral region of said channel, and said second drain portion and said second supplemental gate are located proximate a second lateral region of said channel, and said first supplemental gate is electrically interconnected with said second drain portion, and said second supplemental gate is electrically interconnected with said first drain portion.

3. The device of claim 2, wherein said doped layer is formed of p-type semiconductor material, and said source and drain regions are formed of n-type semiconductor material.

4. The device of claim 2, wherein said doped layer is formed of n-type semiconductor material, and said source and drain regions are formed of p-type semiconductor material.

5. A method of detecting a magnetic field in a split drain field effect transistor comprising a source region, a channel interconnecting said source region to a drain region, first and second drain contacts for guiding current from laterally spaced portions of said channel, said method comprising:

   applying a controlled electric field, laterally across said channel in a direction parallel to the force experienced by electrons in said channel under the influence of a magnetic field.

6. The method of claim 5, wherein said electric field is generated as a result of a current imbalance between said first drain portion and said second drain portion.

7. The method of claim 6, wherein said electric field is applied to said channel by way of two supplemental gates proximate said channel.

8. The method of claim 7, wherein a potential difference across said supplemental gates is generated by said current imbalance.

9. A field effect transistor comprising:

   a semiconductor substrate;

   a source region and a drain region;

   a channel formed in said substrate for guiding current from said source region to said drain region along a lengthwise extent of said channel;

   a gate in proximity with said channel for controlling current from said source to said drain;

   said drain region comprising first and second drain contacts, each of said

first and second drain contacts for guiding current from a lateral portion of said channel;

first and second supplemental gates proximate said channel for establishing an electric field in said channel, in a direction perpendicular to said lengthwise extent.

10. A magnetic latch for detecting an external magnetic field comprising the field effect transistor of claim 9, wherein said first drain contact and said first supplemental gate are located proximate a first lateral region of said channel, and said second drain contact and said second supplemental gate are located proximate a second lateral region of said channel, and said first supplemental gate is electrically interconnected with said second drain contact, and second supplemental gate is electrically interconnected with said first drain contact.

11. A magnetic latch of claim 10, further comprising a reset switch connected between said first supplemental gate and said second supplemental gate, to short said first supplemental gate and said second supplemental gates to reset said device.

12. A magnetic switch comprising the latch of claim 10, wherein said source and said first drain contact are interconnected to an electronic circuit, to switch current through said first drain contact to said electronic circuit in the presence of a magnetic field.

13. A magnetic memory element for storing a unit of binary information, comprising the magnetic latch of claim 10.